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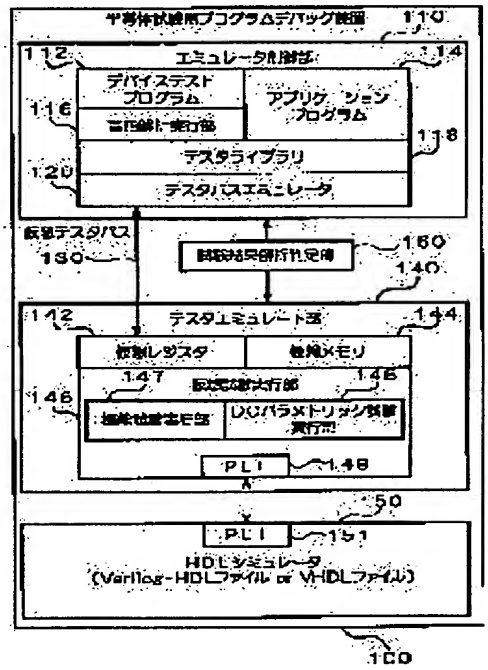
(54) PROGRAM DEBUGGING APPARATUS FOR SEMICONDUCTOR TEST

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain a program debugging apparatus which obtains a test result similar to that in a case where a program for semiconductor test is operated with respect to an actual semiconductor device to be inspected and by which the content of the program for semiconductor test can be verified accurately on the basis of the test result.
SOLUTION: A test emulation part 140 operates a device test program 112 to be an object to be debugged under the operating system of a general-purpose computer, and a semiconductor testing apparatus is constituted in a pseudo manner. An HDL simulation part 150 simulates a semiconductor device on the basis of a file which is described by a hardware description language. The semiconductor device which is simulated by the HDL simulation part 150 becomes an ideal semiconductor device which is operated completely in the same way as a semiconductor device, to be inspected, which does not contain a defect due to its production. A test signal is supplied to the semiconductor device so as to be tested, the test signal is supplied to the ideal semiconductor device so as to be tested equally, and the accuracy of a debugging operation about whether a program for semiconductor test is operated normally can be increased.



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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] A circuit tester emulation means to generate in false the stimulus impressed to the semiconductor device for inspected based on the program for a semi-conductor trial, and to emulate actuation of a semi-conductor testing device, Said semiconductor device for inspected is simulated based on a hardware description language. Said stimulus outputted to said simulated inspected semiconductor device from said circuit tester emulation means is supplied. A hardware description language simulation means to simulate and output the signal outputted from said semiconductor device for inspected according to supply of this stimulus, With said hardware description language simulation means Program debugging equipment for a semi-conductor trial characterized by being constituted including the debugging means which debugs said program for a semi-conductor trial based on the signal outputted from said simulated semiconductor device for inspected.
[Claim 2] It is program debugging equipment for a semi-conductor trial characterized by said hardware description language simulation means simulating said semiconductor device for inspected in claim 1 based on Verilog-HDL as said hardware description language.
[Claim 3] It is program debugging equipment for a semi-conductor trial characterized by said hardware description language simulation means simulating said semiconductor device for inspected in claim 1 based on VHDL as said hardware description language.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the program debugging equipment for a semi-conductor trial which emulates a semi-conductor testing device and performs the program verification for a trial.
[0002]
[Description of the Prior Art] From the former, the semi-conductor testing device is known as what performs a direct-current trial, a functional test, etc. to various kinds of semiconductor devices, such as a logic IC before shipment, and semiconductor memory. The trial which a semi-conductor testing device performs is divided roughly, and are a functional test and a direct-current trial. A functional test gives a predetermined test pattern signal to the semiconductor device for inspected, and inspects whether the semiconductor device for inspected performed prearranged actuation to this test pattern signal. A direct-current trial inspects whether the property which the direct-current property of each terminal of the semiconductor device for inspected planned is fulfilled. For example, when the voltage-source-current-measurement trial which examines whether a prearranged current can take out from a terminal when a known electrical potential difference is impressed, or a known current is passed or taken out, there is a current-source-voltage-measurement trial which examines whether the prearranged electrical potential difference has occurred for the terminal. Moreover, even when performing a functional test, set the electrical potential difference at the time of high level as 4 volts of the electrical-potential-difference value of normal, for example, a value lower than 5 volts, the electrical potential difference at the time of a low level is set as 0.5 volts of the electrical-potential-difference value of normal, for example, a value higher than 0 volt, or it carries out in many cases by changing various electrical-potential-difference conditions impressed to the semiconductor device for inspected, current conditions, etc.
[0003] Since various kinds of conditions of what kind of item to examine on what kind of conditions are beforehand included in the program for a semi-conductor trial when performing a functional test and a direct-current trial, the various trials of the semiconductor device for inspected can be performed by operating this program for a semi-conductor trial. However, the program for a semi-conductor trial must control the actuation across which it goes variably, such as a setup of a trial item, a setup of a test condition, experimental activation, and a judgment of a test result, and is built by the program of a huge step. When the class of semiconductor device for inspected is changed or that logic is changed, this program for a semi-conductor trial is combined with it, and must be changed variously. When the program for a semi-conductor trial is created newly or is changed, the program itself must evaluate the program for whether it is what operates normally. To the semiconductor device for inspected which the quality understands beforehand using the semi-conductor testing device actual as law on the other hand, the program for a semi-conductor trial was operated and the program was evaluated. However, the semi-conductor testing device itself is expensive, evaluating whether the program for a semi-conductor trial operates normally from there being little introductory number using an actual semi-conductor testing device will stop Rhine of a semi-conductor trial,

and it is not desirable. Then, it was verifying whether conventionally, the program for a semi-conductor trial would not be evaluated using an actual semi-conductor testing device, but a semi-conductor testing device would be emulated using general purpose computers, such as a workstation, and the program for a semi-conductor trial would operate normally.
[0004] Thus, there is a thing which was indicated by JP,9-185519,A to emulate a semi-conductor testing device. This is related with the debugging equipment for examining whether the program for a semi-conductor trial operates normally. This constitutes the false semi-conductor testing device by operating the program for a semi-conductor trial which serves as a candidate for debugging under the operating system of a general purpose computer. The examined [virtual] component section, the test condition setting section, the trial item setting section, the test-result storing section, etc. are connected to this false semi-conductor testing device through the interface section, and the false functional test and the direct-current trial are performed by reading the virtual data set as this examined [virtual] component section according to the test condition set as the test condition setting section.
[0005]
[Problem(s) to be Solved by the Invention] By the way, the actual semiconductor device for inspected is not necessarily used for the conventional debugging equipment mentioned above, and it was not able to perform it on a par with the case where the actual semiconductor device for inspected is used for the functional test by the program for a semi-conductor trial. For this reason, when it was going to debug the program for a semi-conductor trial, the transition of logic according to the function of the semiconductor device for inspected and a coincidence inequality with expected value could not fully be judged, and the contents of the program for a semi-conductor trial were not able to be exactly verified as a result.
[0006] This invention is created in view of such a point, and that purpose obtains the same test result as the case where the program for a semi-conductor trial is operated to the actual semiconductor device for inspected, and is to offer the program debugging equipment for a semi-conductor trial which can verify the contents of the program for a semi-conductor trial exactly based on this test result.
[0007]
[Means for Solving the Problem] In order to solve an above-mentioned technical problem, the program debugging equipment for a semi-conductor trial indicated by claim 1 A circuit tester emulation means to generate in false the stimulus impressed to the semiconductor device for inspected based on the program for a semi-conductor trial, and to emulate actuation of a semi-conductor testing device, Said semiconductor device for inspected is simulated based on a hardware description language. Said stimulus outputted to said simulated inspected semiconductor device from said circuit tester emulation means is supplied. A hardware description language simulation means to simulate and output the signal outputted from said semiconductor device for inspected according to supply of this stimulus, It is constituted including the debugging means which debugs said program for a semi-conductor trial based on the signal outputted from said semiconductor device for inspected simulated by said hardware description language simulation means.
[0008] A circuit tester emulation means operates the program for a semi-conductor trial which serves as a candidate for debugging under the operating system of a general purpose computer, and constitutes a semi-conductor testing device in false. A hardware description language simulation means simulates a semiconductor device based on the file described by hardware description languages, such as Verilog-HDL or VHDL. Therefore, by supplying and examining a stimulus to this semiconductor device, since it is the semiconductor device for inspected which does not include the defect by manufacture, and the ideal semiconductor device which completely operates similarly, the semiconductor device simulated by the hardware description language simulation means supplies a stimulus to an ideal semiconductor device, becomes equal to examining, and becomes possible [raising the debugging precision of whether the program for a semi-conductor trial operates normally].
[0009]
[Embodiment of the Invention] Hereafter, the gestalt of 1 operation of the program debugging

equipment for a semi-conductor trial concerning this invention is explained, referring to a drawing. Drawing 1 is drawing showing the whole program debugging equipment configuration for a semi-conductor trial. By emulating actuation of a semi-conductor testing device, and simulating actuation of the semiconductor device for inspected, debugging equipment 100 is for verifying whether the program for a semi-conductor trial operates normally, and is realized by general purpose computers, such as a workstation.

[0010] Since the debugging equipment 100 concerning the gestalt of this operation simulates actuation of an actual semi-conductor testing device and the semiconductor device for inspected, before it gives that detailed explanation, it explains the configuration of the semi-conductor testing device simulated.

[0011] Drawing 2 is drawing showing the actual semi-conductor testing-device whole configuration. The condition that the actual semiconductor device 250 for inspected was connected to the semi-conductor testing device 200 is shown by this drawing. The semi-conductor testing device 200 performs various kinds of direct-current trials (DC parametric trial) and functional tests to the semiconductor device 250 for inspected. The semi-conductor testing device 200 is constituted including the socket section (not shown) which carries the circuit tester control section 210, the circuit tester bus 230, the circuit tester body 240, and the semiconductor device 250 for inspected.

[0012] The circuit tester control section 210 is for controlling actuation of the circuit tester body 240, and is constituted including the program 212 for a semi-conductor trial (device test program), an application program 214, the language analysis activation section 216, the circuit tester library 218, and the circuit tester bus driver 220.

[0013] The device test program 212 describes the procedure and approach for what kind of trial a user performs to the semiconductor device 250 for inspected using the semi-conductor testing device 200. Generally development creation of this device test program is done by the user of the semi-conductor testing device 200. Therefore, without using the actual semi-conductor testing device 200, a user can verify whether the device test program 212 which he created using the debugging equipment 100 concerning the gestalt of this operation operates normally, and can create a highly complete device test program. The language analysis activation section 216 performs syntax analysis of the device test program 212 etc., and plays the central role which operates the semi-conductor testing device 200 faithfully according to the device test program 212. An application program 214 cooperates with the device test program 212 and the language analysis activation section 216, operates, impresses the actual stimulus corresponding to a functional test and a direct-current trial etc. to the semiconductor device 250 for inspected, incorporates the output signal, and the quality of the semiconductor device 250 for inspected is judged, or it analyzes a property. The circuit tester library 218 directs measurement actuation to the circuit tester body 240 while it changes the instruction of the device test program 212 after syntax analysis was performed by the language analysis activation section 216 into the instruction (data about the data write-in instruction to the register 242 mentioned later, and the data read-out instruction from a register 242) of register level and performs creation and a setup of data required for actuation of the semi-conductor testing device 200. The circuit tester bus driver 220 transmits the data created by the circuit tester library 218 to the register 242 within the circuit tester body 240 through the circuit tester bus 230.

[0014] The circuit tester body 240 performs various kinds of trials to the semiconductor device 250 for inspected based on the data from the circuit tester control section 210 incorporated through the circuit tester bus 230. The circuit tester body 240 is constituted including a register 242, memory 244, and the test activation section 246. A register 242 stores the data from the circuit tester library 218 incorporated through the circuit tester bus 230. The data stored in this register 242 are outputted to the test activation section 246 through direct or memory 244. Moreover, a register 242 and memory 244 have the test-result storing field (not shown) which stores the data about the test result from the test activation section 246.

[0015] The test activation section 246 is equipped with the functional test activation section 247 and the DC parametric test activation section 248. Based on the data from the circuit tester

library 218 stored in a register 242 or memory 244, the test activation section 246 performs a functional test and DC parametric trial to the semiconductor device 250 for inspected, and stores the data of the test result in the test-result storing field of a register 242 or memory 244. The test-result data stored in a register 242 and memory 244 are incorporated by the circuit tester driver 220 to the direct circuit tester library 218 through the circuit tester bus 230. In addition, the test-result data stored in memory 244 are incorporated to the circuit tester library 218 through a register 242.

[0016] The debugging equipment 100 of drawing 1 simulates actuation of the semiconductor device 250 for inspected while emulating the above-mentioned actuation by the whole semi-conductor testing device 200. Therefore, if the device test program 112 created for the semi-conductor testing devices 200 is performed using the debugging equipment 100 of drawing 1 , actuation of the device test program 112 can investigate whether it is in agreement with what the user meant. Next, the configuration of the debugging equipment 100 concerning the gestalt of this operation is explained.

[0017] The emulator control section 110 shown in drawing 1 is constituted including the device test program 112, an application program 114, the language analysis activation section 116, the circuit tester library 118, and the circuit tester bus emulator 120. This emulator control section 110 is for controlling actuation of the circuit tester emulation section 140, and performs the same actuation fundamentally with the circuit tester control section 210 contained in the semi-conductor testing device 200 shown in drawing 2 .

[0018] The device test program 112 is a program which describes the procedure and approach for what kind of trial is performed to the semiconductor device 250 for inspected using the semi-conductor testing device 200, and is set as the object of debugging with debugging equipment 100. Therefore, the device test program 212 of drawing 2 is transplanted as this device test program 112 as it is, and it is constituted so that same actuation may be performed. The application program 214, the language analysis activation section 216, and the test library 218 of drawing 2 are similarly transplanted as it is about an application program 114, the language analysis activation section 116, and the circuit tester library 118, and it is constituted so that same actuation may be performed. The circuit tester bus emulator 120 drives the virtual circuit tester bus 130 which connects virtually between the emulator control section 110 and the circuit tester emulation sections 140, and controls transmission and reception of the data between the circuit tester library 118 and the circuit tester emulation section 140 through this virtual circuit tester bus 130.

[0019] The circuit tester emulation section 140 realizes actuation of the circuit tester body 240 of drawing 2 by software, and performs the simulation-trial to the hardware description language (HDL) simulator 150 according to directions of the circuit tester library 118 in the emulator control section 110 of operation. The circuit tester emulation section 140 is constituted including the virtual register 142, virtual memory 144, and the virtual test activation section 146. The virtual register 142 stores the data from the circuit tester library 118. The data stored in this virtual register 142 are sent to the virtual test activation section 146 through direct or virtual memory, 144. Moreover, the virtual register 142 and virtual memory 144 have the test-result storing field (not shown) which stores the virtual test-result data outputted from the virtual test activation section 146.

[0020] The virtual test activation section 146 is equipped with the functional test activation section 147 and the DC parametric test activation section 148. Based on the data from the circuit tester library 118 stored in the virtual register 142, this virtual test activation section 146 outputs a predetermined signal to the HDL simulation section 150, performs the functional test by the functional test activation section 147, and DC parametric trial by the DC parametric test activation section 148, and stores that virtual test-result data in the test-result storing field of the virtual register 142 or virtual memory 144. The virtual test-result data stored in the virtual register 142 and virtual memory 144 are outputted to the circuit tester library 118 through the virtual circuit tester bus 130. The test-result analysis judging section 160 carries out comparison examination of the virtual test-result data stored in the virtual register 142, virtual memory 144, or the circuit tester library 118, and the expected value of the test result expected, verifies

whether the device test program 112 is operating normally, and displays the result on a user. For example, when the test result which was mistaken with activation of the device test program 112 is obtained, the program line number leading to the mistaken test result etc. is displayed on a monitor (not shown), or is printed by the printer (not shown).
[0021] Next, actuation of the circuit tester emulation section 140 is explained. If access to the virtual register 142 from the virtual circuit tester bus 130 enters, based on the address of the virtual register 142, the access calculates whether it is access to the part of virtual register 142 throat, data will be written in the location or the circuit tester emulation section 140 will read data from the location to it. Moreover, to the virtual memory 144 of a proper, data will be written in or the circuit tester emulation section 140 will read data, if access to virtual memory 144 arises through access of the virtual register 142. In this case, generally sufficient information to write data to virtual memory 144 cannot be acquired only with one virtual register 142. So, with the gestalt of this operation, the circuit tester emulation section 140 is made to perform the R/W of data to virtual memory 144 with reference to the contents of the related virtual register 142. In addition, in the case of debugging equipment 100, when performing the same processing as the semi-conductor testing device 200 of drawing 2 , although the virtual test-result data stored in virtual memory 144 will be outputted to the circuit tester library 118 through the virtual register 142 and the virtual circuit tester bus 130, they may be constituted so that the virtual test result stored in virtual memory 144 may be outputted to the direct circuit tester library 118.

[0022] When the register which starts wave-like generating (functional test) is accessed to the circuit tester emulation section 140, in the 1st task, wave-like generating processing by the virtual test activation section 146 is performed. Since the required data about wave generating are beforehand stored in the virtual register 142 and virtual memory 144 at this time, the virtual test activation section 146 generates a wave, referring to it. The wave generated by the virtual test activation section 146 is transmitted to the HDL simulation section 150 through the programming language interface (PLI:Programing Language Interface) 149,151. The HDL simulation section 150 simulates the completely same actuation as the actual semiconductor device 250 for inspected based on the inputted wave. The output pin data of the result simulated by the HDL simulation section 150 are again fed back to the virtual test activation section 146, it is compared with expected value there, and the result is stored in the predetermined virtual register 142 and virtual memory 144. Executive operation of a series of above-mentioned actuation is carried out for every operating cycle of the circuit tester emulation section 140.
[0023] The HDL simulation section 150 simulates the semiconductor device based on the file described by hardware description languages, such as Verilog-HDL or VHDL. That is, since the HDL simulation section 150 is simulating the semiconductor device of the product itself based on the Verilog-HDL file or VHDL file at the time of the design of the actual semiconductor device 250 for inspected shown in drawing 2 , the simulated semiconductor device turns into the semiconductor device 250 for inspected, and an ideal semiconductor device which completely operates similarly, without including the defect by manufacture. Therefore, the circuit tester emulation section 140 will examine to such an ideal semiconductor device. In addition, between the HDL simulation section 150 and the virtual test activation section 146, it connects through the programming language interface 149,151, and the exchange of a stimulus and a test result is performed.
[0024] In addition, without carrying out, paying attention to the property of a circuit tester, timing data and a wave format are made to Maine, and simulating the logic components which constitute a circuit tester one by one has made the data point by 1 cycle in the event format, and it supplies the circuit tester emulation section 140 to the HDL simulation section 150. The HDL simulation section 150 simulates the logic components which constitute it one by one with an event driven method, and it performs them until 1 circuit-tester cycle is completed. And holding the internal state, when 1 circuit-tester cycle was completed, a simulation is closed and the output change in the cycle is transmitted to the circuit tester emulation section 140 in an event format. The circuit tester emulation section 140 analyzes again the output change for 1 cycle from the HDL simulation section 150, and stores the judgment result of pass/fail in the

virtual register 142 or virtual memory 144 as compared with expected value. By performing such actuation, the effectiveness of wave generating of the circuit tester emulation section 140 becomes good. Moreover, since data are processed for every cycle, data transfer effectiveness becomes good. Moreover, depending on the case, two or more cycles may be processed collectively.

[0025] The hardware description language simulation section 150 corresponds to a HDL simulation means, and the test-result analysis judging section 160 corresponds [the emulator control section 110 and the circuit tester emulation section 140 which were mentioned above] to a circuit tester emulation means at a debugging means, respectively.

[0026] Actuation of the debugging equipment 100 of drawing 1 is explained using a drawing. Drawing 3 is the flow chart showing the operations sequence of the debugging equipment 100 at the time of performing the device test program 112 for a direct-current trial (DC parametric trial) or functional tests. This flow starts processing, when a user directs debugging actuation of the device test program 112. First, the device test program 112 set as the object of debugging actuation at step 100 is performed. Next, the language analysis activation section 116 in the emulator control section 110 analyzes syntax of the device test program 112 at step 101. After syntax analysis is performed by the language analysis activation section 116, the circuit tester library 118 changes the instruction of the device test program 112 into the instruction of register level at step 102, data required for actuation of debugging equipment 100 are created based on it, and these data are stored in the virtual register 142 in the circuit tester emulation section 140. After storing of the data to the virtual register 142 is completed, the emulator control section 110 directs measurement actuation to the circuit tester emulation section 140 at step 103.

[0027] The circuit tester emulation section 140 which received directions of measurement actuation from the emulator control section 110 performs a false functional test or a direct-current trial (DC parametric trial) to the HDL simulation section 150 according to directions of the circuit tester library 118 in the emulator control section 110 of operation. Specifically, the functional test activation section 147 in the virtual test activation section 146 or the DC parametric test activation section 148 outputs the predetermined stimulus based on the data stored in the virtual register 142 to the HDL simulation section 150 according to directions of the circuit tester library 118 in the emulator control section 110 of operation at step 104. At step 105, the HDL simulation section 150 impresses a stimulus to the semiconductor device for inspected simulated based on the Verilog-HDL file or the VHDL file, performs a functional test or a direct-current trial (DC parametric trial), and outputs the measured value corresponding to the test result. If measured value is outputted from the HDL simulation section 150, the functional test activation section 147 or the DC parametric test activation section 148 is stored in the virtual register 142 or virtual memory 148 by using this measured value as virtual test-result data at step 106. The virtual test-result data stored in the virtual register 142 or virtual memory 148 are outputted to the circuit tester library 118 in the emulator control section 110 at step 107, and the circuit tester library 118 performs predetermined processing corresponding to this virtual test-result data.

[0028] In addition, since it is described beforehand what kind of actuation is performed to the device test program 112 corresponding to various measurement results, if a programmer means [the processing which the circuit tester library 118 performs corresponding to virtual test-result data], it will be verified that there is no error in the applicable part of the device test program 112. On the contrary, if the processing which the circuit tester library 118 performs corresponding to virtual test-result data is not what the programmer meant, it will be verified that an error is in the applicable part of the device test program 112. Thus, debugging actuation of the device test program 112 is performed.

[0029] Thus, the HDL simulation section 150 The semiconductor device is simulated based on the Verilog-HDL file or VHDL file at the time of the design of the actual semiconductor device 250 for inspected. Since it will examine to an ideal semiconductor device without a manufacture error or a manufacture defect There is less variation than the case where the semiconductor device for inspected of the actually manufactured excellent article is used, the actuation at the

time of a trial can be emulated exactly, and it becomes possible to raise the precision of debugging of the device test program 112.
[0030] Moreover, although the debugging equipment 100 which debugs the device test program which examines the semiconductor device 250 for inspected was considered with the gestalt of operation mentioned above, as a class of semiconductor device for inspected, various things, such as semiconductor memory specified by a Verilog-HDL file or the VHDL file, various kinds of processors, and IC for logic, can be considered.
[0031] In addition, although the gestalt of above-mentioned operation explained the case where a semiconductor device was simulated based on the Verilog-HDL file or VHDL file at the time of the design of the actual semiconductor device for inspected, you may make it simulate a semiconductor device using the Verilog-HDL file or VHDL file specially created to program debugging for a semi-conductor trial.
[0032] Moreover, although the gestalt of above-mentioned operation explained the case where the program for a semi-conductor trial was debugged, you may make it debug a Verilog-HDL file or a VHDL file by examining the semiconductor device simulated based on the Verilog-HDL file or the VHDL file using the formal program for a semi-conductor trial.
[0033]
[Effect of the Invention] As mentioned above, the test result same according to this invention as the case where the program for a semi-conductor trial is operated to the actual semiconductor device for inspected is obtained, and it is effective in the contents of the program for a semi-conductor trial being exactly verifiable based on this test result.

[Translation done.]

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is drawing showing the whole debugging equipment configuration of this operation gestalt.
[Drawing 2] It is drawing showing the whole semi-conductor testing-device configuration.
[Drawing 3] It is the flow chart showing the operations sequence of the debugging equipment at the time of performing a device test program.
[Description of Notations]
100 Debugging Equipment
110 Emulator Control Section
112 Device Test Program
140 Circuit Tester Emulation Section
146 Virtual Test Activation Section
147 Functional Test Activation Section
148 DC Parametric Test Activation Section
150 HDL Simulation Section
149,151 Programming language interface
160 Test-Result Analysis Judging Section

[Translation done.]